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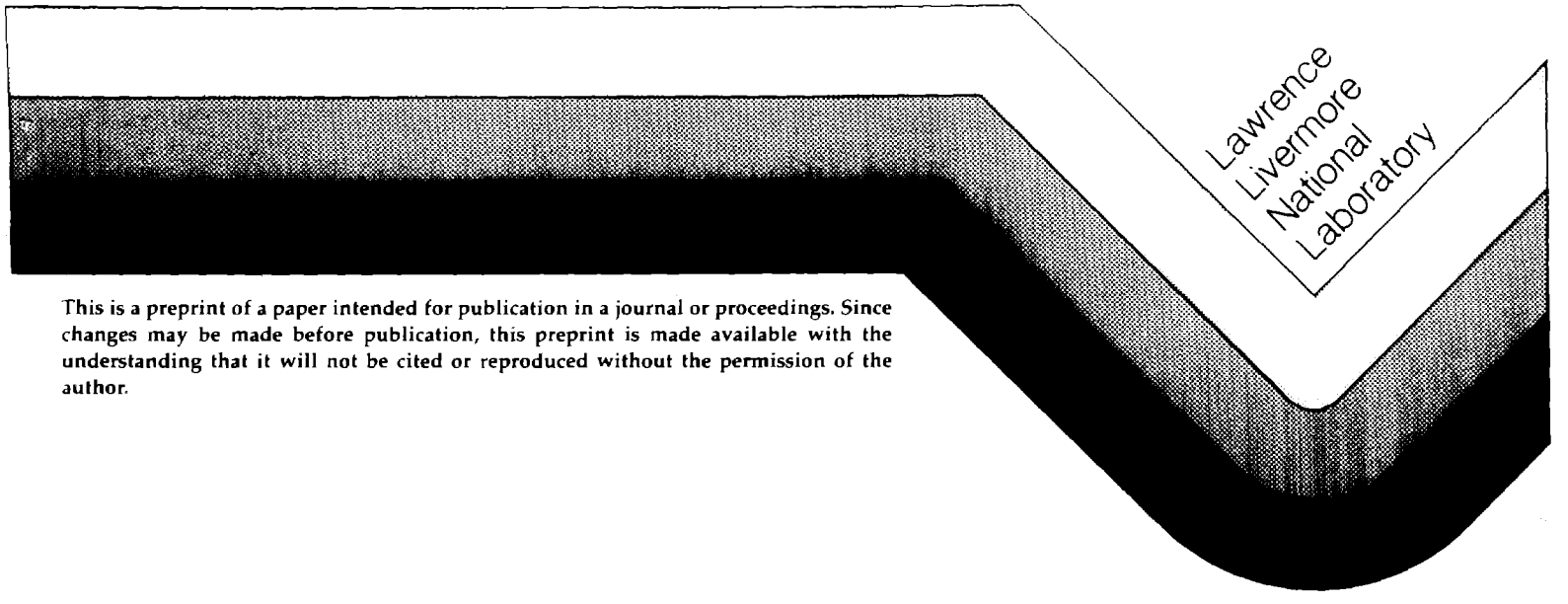

A SUB-200 PICOSECOND GaAs SAMPLE-AND-HOLD CIRCUIT FOR A MULTI-GIGASAMPLE/SECOND INTEGRATED CIRCUIT*

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ABSTRACT

We report initial results on a digital/analog, 1-micron gate GaAs MESFET IC whose purpose is to record with bandwidths exceeding 1 GHz non-repetitive analog transient waveforms of a few nanoseconds duration. Specialized buffered-fet logic digital circuits with T_{pd} as low as 70 psec generate a pulse burst that strobe a series of 20 linear gate sample-and-hold circuits. These 3-gate MESFET sampling circuits have demonstrated sampling apertures of less than 200 psec, without pretriggering required. Backgating effects on the circuit design and performance and high speed techniques are reviewed. Earlier work (1) on this scheme has been extended from 1nsec step inputs to 100 psec and variable biasing in the linear gate circuit has been added.

INTRODUCTION

Many high energy physics experiments at our laboratory and others that frequent the pulse power domain generate diagnostic electronic recording requirements for non-repetitive, high-bandwidth transient waveforms. Current real-time oscilloscopes are limited to about 1 GHz, or 350 psec equivalent risetime, and often this is insufficient. Furthermore, for many destructive experiments, such as explosive testing, the destruction of the sensors and the oscilloscope shortly after triggering precludes its use because of cost and/-or insufficient time to readout or transfer the recording to a remote data acquisition system. While streak tubes have resolutions below 10 psec, they suffer the limitations of optical input/output, calibration difficulties, and great expense in addition to the limitations imposed upon oscilloscopes. Sampling rates of 2-5 Gigasamples/sec and record lengths of several hundred samples are highly desirable, although many experiments become possible with record lengths of 50-100 samples; basic waveform features can be determined with this modest number of samples and with modest accuracies of 7-8 bits resolution. Current commercially available A-to-D chips are predominantly designed for CW operation and operate well below 0.5 Gigasamples/sec and/or have less than 7 bit resolution. Our GaAs IC is designed to operate in the 3-5 Gigasample/sec range with 7 bit resolution and be integrable to about 100 sample record length; it is especially designed for single-shot or very low duty cycle operation.

The complete waveform recording system uses a double sample-and-hold technique with GaAs for the first stage with storage times of about 10 microseconds, followed by an inexpensive commercially available second stage silicon sample-and-hold IC for each sample point. The different sample points are then multiplexed sequentially into a 12 bit silicon A-to-D chip and the recording is completed in a few milliseconds.

FABRICATION

Our GaAs IC processing utilizes undoped 2 inch diameter LEC substrates and seven masking levels. The n-channels are formed by localized Si^{29} implantation of $2.5E12cm^{-2}$ at both 60 keV and 200 keV. Capless, face-to-face annealing is done at 850°C/30 min in argon with polycrystalline InAs serving as an arsenic vapor source to reduce the loss of arsenic from the GaAs. Ohmic contacts are formed by depositing Au-Ge eutectic/Ni/Au (500 A°/50 A°/1000 A°) onto the $n^+(2.5E13cm^{-2})$ implant regions and then alloying in argon at 400°C for 45 seconds. A gate recess etch (40:1 mix 50 percent wt citric acid and 30 percent H_2O_2 at 0°C for 4-5 minutes) sets the pinchoff voltage of our depletion mode MESFETS to about -2.0 volts. Cr/Au (20 A°/3000 A°) gates one micron long are used with one micron gate-to-source gaps or gate-to-gate gaps. Cr/Au 5 micron wide interconnects are used with one micron thick polyimide for the dielectric, which is also used for the on-chip storage or holding capacitors and the RF by-pass capacitors. Ohmic alloy metal, followed by first level interconnect metal, forms the bottom plate of the 0.35 pf storage capacitors; the top plate is the second level interconnect metal. Three micron via holes are oxygen plasma etched through the polyimide and produce 45 degree sidewalls for excellent step coverage. The only critical processing step is the Schottky gate formation. The photoresist exposure is less tolerant than usual because of proximity effects on the 3 gate sample MESFETS that are exposed at the same time as the single gate FETS. The gate recess etch step is also sensitive and it removes about 750-1000 A° of the GaAs. The first few hundred Angstroms of the GaAs seems to implant convert very poorly compared to the main part of the channel (>75 percent conversion) and we suspect that arsenic loss and surface damage may be contributing factors.

The standard 20 micron wide MESFETS have g_m=4ms(200 mS/mm), V_p=-2.0 volts, $\sigma(V_p)$=11 percent on 1cm^2, contact resistance of 7.5 ohms, and breakdown voltage greater than 18 volts. The addition of the InAs arsenic source to the implant annealing has greatly reduced our backgating effect from its previously severe value (> 50 percent at -8V) to that shown in Figure 1; this backgating effect ranges from negligible (< 2 percent) to small (< 13 percent) and tolerable for our circuit designs. The spread in backgating shown in Figure 1 is typical over one wafer lot that was annealed together; the source material was from 4-5 adjacent 2 inch diameter wafers from the same boule.

CIRCUIT DESIGN

The 20-sample, single-analog-input IC circuit is shown in Figure 2. The trigger pulse starts a step pulse that propagates through the inverter string where the gate delays are about T_{pd}=100 psec. The AND gates form a series of strobe pulses very 2 T_{pd} with a pulse width of 3 T_{pd}; thus the sampling rate can be as high as 5 Giga-samples/sec. Each AND gate forms one strobe pulse that turns on the 3-gate sampling FET in the sample-and-hold circuit shown in the inset to Figure 2. The strobe pulse width of 3 T_{pd} is not the limiting factor because the holding capacitor, C_s, tracks the analog input with a time constant significantly less than 2 T_{pd}. The on-resistance of the 3-gate FET is about 50 ohms and the 0.3 pf storage capacitor leads to an RC time constant of 15 psec; the transit time of the 3-gate FET is estimated to be about 15-20 psec. Thus the voltage on the storage capacitor tracks the analog input fairly quickly until the strobe pulse falls. The 3-gate FET should turn off in some fraction of the actual fall time--perhaps one-half. The on-chip generated strobe pulse is estimated to have a fall time of about 120 psec; the externally generated strobe test pulse on the test structure reported below had a fall time of 200 psec. Thus, the aperture time or the sampling interval is estimated to be in the range of 60-100 psec.

The side gates of the 3-gate FET serve to significantly reduce strobe pulse feedthrough onto the storage capacitor as demonstrated previously (1). Our side gates have an adjustable bias and are capacitively RF by-passed to ground close to the sampling FET. The optimum holding time occurs at a side gate bias of about -1V and it is 25 microseconds. The quiescent voltage on the storage capacitors varies considerably as determined by leakage currents in the semi-insulating substrate to ground and from the source follower and the 3-gate FET; these currents vary from circuit to circuit. The signal voltage on the storage capacitor is read out in a few microseconds, before it can decay to its quiescent value, by a silicon sample-and-hold circuit via the source follower. The output signal rises above a DC baseline offset level of about 1 volt. In order to insure the backgating would not reduce the source followers saturated current to less than the current sink value, the source FET width is 4 times that of the sink FET. This insures low current leakage loads caused by the source follower on the storage capacitor but introduces the base line offset voltage at the output. The input/output transfer function, including the baseline offset, for each sampler circuit on the chip is recorded by the readout computer during calibration and thus sampler circuit differences, nonlinearities, and offset can be computationally removed after the waveform has been recorded.

This circuit is intended to work in a very high EMI environment so the logic swing of 3 volts was chosen for large noise margins; the logic high and low are +0.4V and -2.6V, respectively. The digital circuits and the analog circuits have separate power busses and they use distributed on-chip RF by-pass capacitors. The input analog signals are over one volt; the output signal of the GaAs chip is about 0.6 volts. The adjacent silicon readout circuits use differential amplification to raise the signals to 10 volts before they are multiplexed and digitized. The switch FET width in the inverter circuits is 20 microns; the BFL logic circuits have level shift diodes with twice the usual width, to provide better drive capability with less series resistance. This change required four level shift diodes. The AND gate shown in Figure 2 is actually a 20 micron wide NAND gate followed by a 40 micron wide driver-inverter with five level shift diodes to insure a sufficiently negative baseline on the strobe pulses so that the sampling FET will be strongly pinched off.

Although the sampling times are not determined by a system clock, the sample time jitter should be an acceptable few picoseconds. The ideal, intrinsic large-signal switching time of the inverter FET has been modeled to be 11 psec. The inverter circuit is dominated by parasitic and load capacitances as shown by Chang (2). The sampling interval should be influenced little by random factors and is dominated by the circuit design (FET widths) and geometrical layout.

The circuit layout placed the ground buss between the parallel plus buss (+5V) and the minus buss (-5V) where possible to minimize the backgating effects that might be introduced by the negative buss. We have experimentally confirmed that intervening grounded electrodes can significantly reduce backgating effects and use this effect frequently as a layout principle.

The analog input signal buss was constructed to appear like a transmission line about 60 psec long with the 3-gate sampling FETs functioning as spatially periodic capacitive loads that are also time dependent. Initial estimates indicate that a better tradeoff could be made by minimizing the signal buss line capacitance further and by using small width sampling FETs. The tracking time constant of the sampling FET would increase. The optimal choice is not clear and would be partially determined by geometrical parasitic layout capacitances that are difficult to model.

PERFORMANCE

The 20 sampler die is shown in Figure 3; the central two-thirds of the die is the inverter string, surrounded by the NAND and driver-inverter gates. On either side of the central digital portion are the sample-and-hold circuits. All the sub-circuits have been tested with the high speed test fixture shown in Figure 4; bondwire taps on the re-entrant strobe and analog truncated microstrip lines take signals to the two separate sample-and-hold sub-circuits on the right edge of the die. Initial results will focus on the performance of the sampler sub-circuits, as they are the key element of this system. Figure 5 shows a dynamic linearity test; strobe pulses of 2.5 to 4 volts worked well. The transfer function (dots) is a smooth parabolic like curve and a least-squares straight line fit to the data is shown in Figure 5. Another circuit simultaneously tested 3 mm distant, had a similar transfer function, with the difference less than 10 percent. Figure 6 shows the externally generated strobe test pulse whose 200 psec fall time limited the present test results. For these sample sub-circuit tests, the delay between the strobe and analog test waveform was manually adjusted; the tests were performed at a few kHz and in single-shot mode with no difference observed. The results in Figures 7-9 compare the analog test waveform (normalized solid line) with the sampler output (dots). With just baseline offset substracted, and no attempt to unfold non-linearities, the sampler circuit can track 100 to 200 psec rise or fall time features on the analog waveform. The present test fixture capacitively couples some of the strobe pulse into the analog signal but the bond wires were too long and the test fixture/chip layout was from from optimal. This fixture was used to test many different sub-circuits and test circuits and can dissipate four watts. Some slight capacitive loading of the fastest analog signal of Figure 9 was evident; it should be noted that in Figure 9, the shape and width (200 psec) of the strobe and analog waveforms were very similar, so the pulse broadening exhibited by the sampler circuit is not suprising. Testing of the full die may require an input compensation network to accommodate the additional capacitive loading. The prototype double sample-and-hold readout channel has been successfully tested, digitized, and read into a computer without signal degradation.

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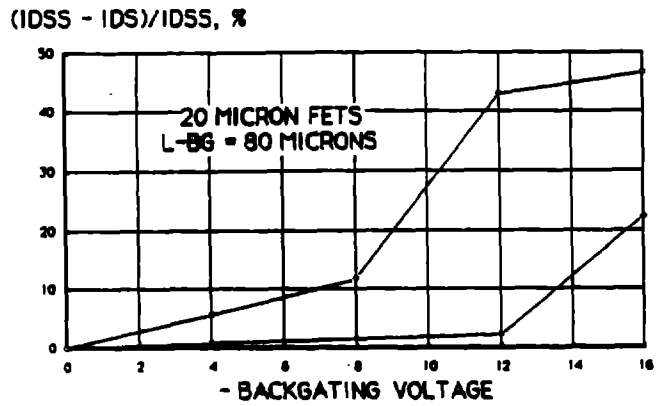

Figure 1. Typical backgating effects on MESFET drain saturation current.

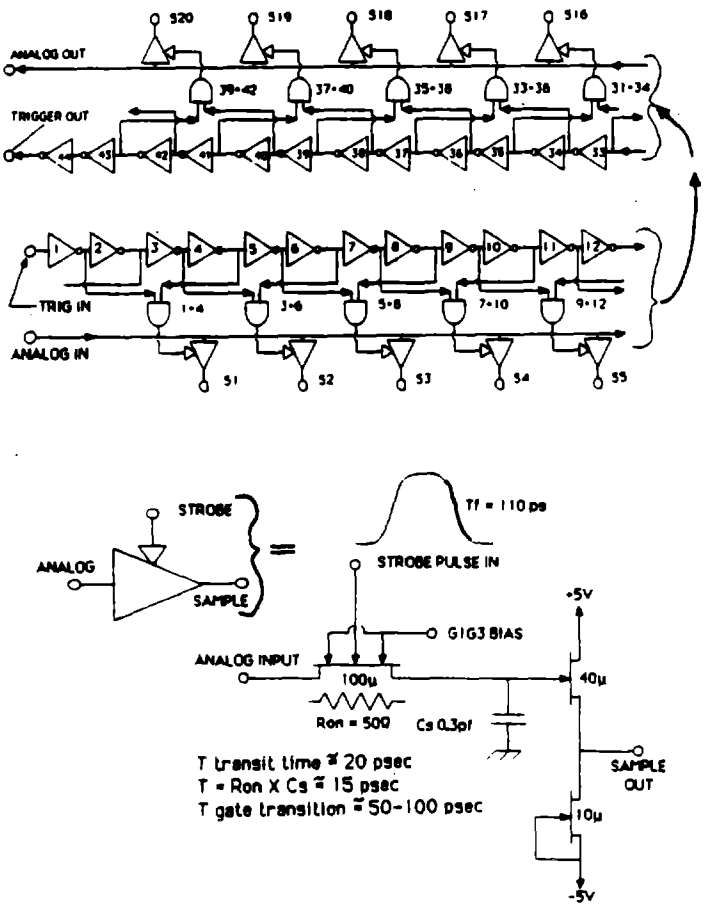

Figure 2. GaAs Sample-and-Hold Circuit τ_{pd} typically = 100 psec.

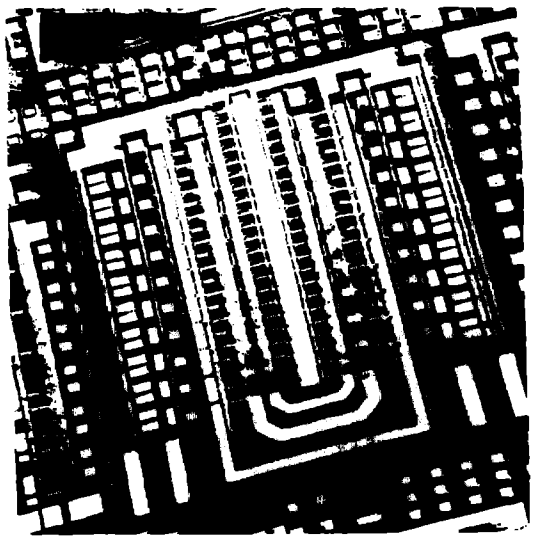

Figure 3. Die size is 3.1 x 3.6 mm^2.

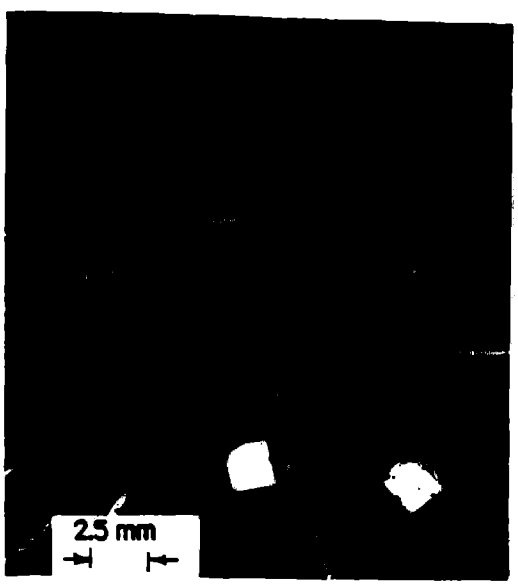

Figure 4. Truncated micro-strip test jig for 2 S&H channels on die edge.

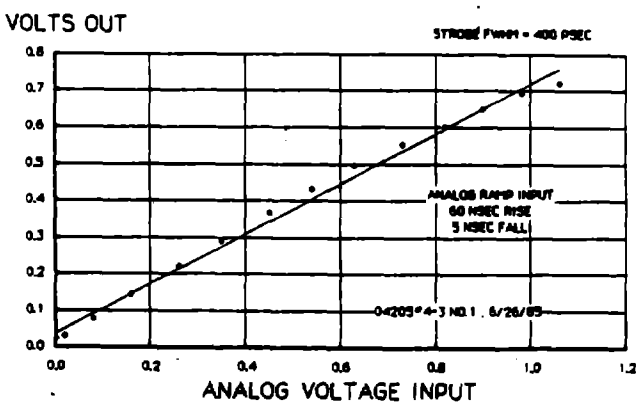

Figure 5. Sampling gate linearity test.

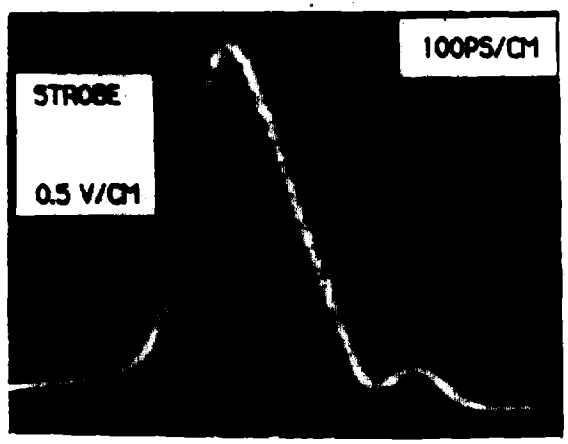

Figure 6. Strobe pulse -3V to 0V, FWHM = 200 psec.

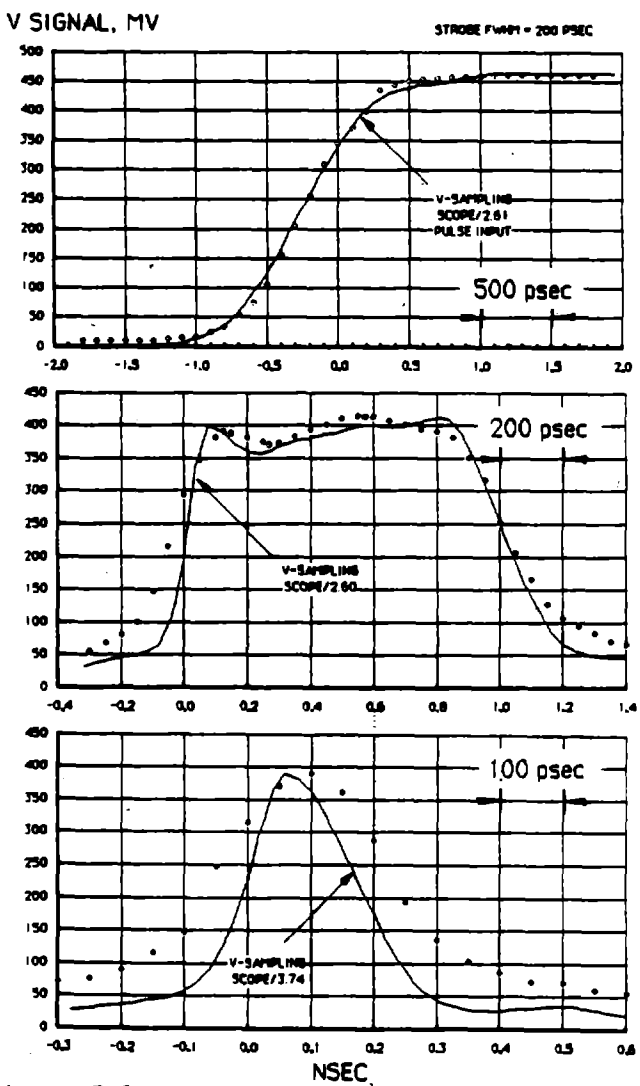

Figure 7-9. Sampler circuit output signal (dots) versus strobe time compared to normalized input analog waveform.